A Network-Flow Based Pin-Count Aware Routing Algorithm for Broadcast-Addressing EWOD Chips

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***Abstract*—Electrowetting-on-dielectric (EWOD) chips have emerged as the most widely used actuators for digital microfluidic (DMF) systems. These devices enable the electrical manipulation of microfluidics with various advantages, such as low power consumption, flexibility, accuracy, and efficiency. In addressing the need for low-cost and practical fabrication, pin-count reduction has become a key problem to the large-scale integration of EWOD-chip designs. One of the major approaches, broadcast addressing, reduces the pin count by assigning a single control pin to multiple electrodes with mutually compatible control signals. Most previous studies utilize this addressing scheme by scheduling fluidic-level synthesis on pin-constrained chip arrays. However, the associated interconnect routing problem is still not provided in currently available DMF automations, and thus the broadcast-addressing scheme cannot be actually realized. In this paper, we present the *first* network-flow based pin-count aware routing algorithm for EWOD-chip designs with a broadcast electrode-addressing scheme. Our algorithm simultaneously takes pin-count reduction and wirelength minimization into consideration for higher integration and better design performance. Experimental results show the effectiveness and scalability of our algorithm on a set of real-life chip applications.**

***Index Terms*—Broadcast-addressing biochips, network flow, printed circuit board, routing.**

I. Introduction

DUE TO THE principle of electrowetting-on-dielectric (EWOD), the EWOD chip has been appreciated as a promising actuator for digital microfluidic (DMF) systems [15], [22], [24], [25]. This chip enables the electrical manipulation of discrete fluidics (i.e., *droplets*) with low power consumption, flexibility, and efficiency. Furthermore, their capability of automatic and parallel controls offers faster and more precise execution. These advantages increase the practicality of applications including immunoassays, DNA sequencing, and point-of-care diagnosis on miniaturized DMF systems with lower cost, less reagent consumption, and higher immunity to human error.

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As schematically presented in Fig. 1(a), the general diagram of a 2-D EWOD chip contains a patterned electrode array, conduction wires, electrical pads (i.e., I/O ports), and a substrate [13], [24], [25]. Through these electrical devices, external micro-controller can drive these electrodes by assigning time-varying actuation voltage. Thus, by generating electrohydrodynamic force from electrodes, many fluidic-level controls can be performed due to the electrowetting phenomenon [22].

In order to drive the electrodes correctly, electrode addressing is introduced as a method through which electrodes are assigned or controlled by pins to identify input signals. Specifically, the external micro-controller reads pin-actuation status from memory, translates them into voltage control signals, and activates or deactivates the corresponding control pins on the EWOD chip [15]. Early EWOD-chip designs relied on direct addressing [13], where each electrode is directly and independently assigned by a dedicated control pin. This addressing maximizes the flexibility of electrode controls. However, due to the limited number of signal ports in the micro-controller, it is infeasible for a micro-controller to activate a large number of control pins. For example, the micro-controller for a recently developed n-plex bioassay application can only activate 64 control pins [4]. Therefore, it cannot control thousands of electrodes directly. Moreover, the high pin-count demand also introduces electrical-connection problems, such as infeasible wiring or multilayer connections. In this regard, it is unreliable and prohibitively expensive to manufacture this kind of chip [27], [28].

Recently, pin-constrained design has been raised as a possible solution to this problem. One of the major approaches, broadcast addressing, reduces the number of control pins by assigning a single control pin to multiple electrodes with mutually compatible control signals [27]. In other words, multiple electrodes are controlled by a single control signal and are thus driven simultaneously. In this regard, much on-going effort has been made to group sets of electrodes that can be driven uniformly without introducing signal conflict [26], [27].

For electrical connections, conduction wires must be routed from the topside electrode array, through the underlying substrate, to the surrounding pads.[1] Hence, after the electrodes are addressed with control pins, the routing problem for EWOD chips can be specified to a 2-D pin array, while establishing correspondence between control pins and pads [see Fig. 1(b)].

[1] In this paper, the routing refers to the wire routing of EWOD chips, which is different from the droplet routing [15], [25].

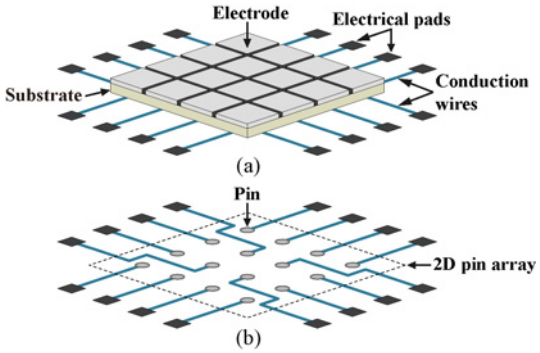


Fig. 1. (a) Schematic view of an EWOD chip. (b) Routing model on a 2-D pin array.

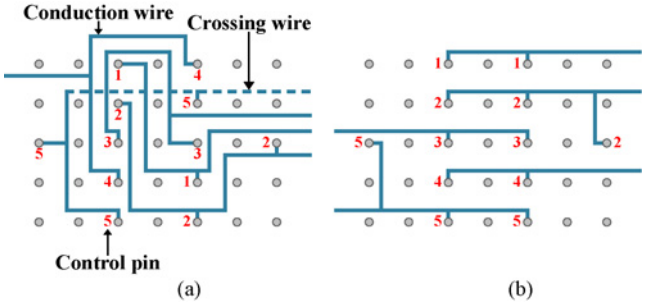


Fig. 2. Comparison of two different design methods for performing the same fluidic controls. (a) Considers electrode addressing and routing separately. (b) Considers electrode addressing and routing simultaneously.

However, this routing issue is still not readily available among automations for EWOD chips, revealing an insufficiency of current DMF design tools. Due to the specialized electrode structure and control mechanism, it is desirable to develop a dedicated routing algorithm for EWOD chips, especially given the issue of the pin-constrained design.

In pin-constrained design, the most critical routing problem for EWOD chips comes from a feature of multiple broadcast-addressing results. Different broadcast-addressing results lead to different wiring connections. If broadcast addressing and routing cannot be converged to an integrated design, the feasibility and quality of the routing solution may be inevitably limited. For example, Fig. 2 illustrates two routing solutions under two different design methods that perform the same fluidic controls. In Fig. 2(a), the separate consideration of electrode addressing and routing confronts many back detours for pins 3–4, and thus blocks the routing for pin 5. On the other hand, in Fig. 2(b), simultaneous consideration of electrode addressing and routing provides a higher feasibility and quality routing solution in terms of routability and wirelength. In the case of Fig. 2(a), additional post processes such as electrode readdressing and rerouting should be further included, and thus the effectiveness of the entire design may be quite restricted.

Given these concerns, it is necessary to develop an integrated design automation to assist in these practical design issues. Consequently, we propose in this paper a pin-count aware routing algorithm that simultaneously considers electrode addressing and routing to achieve greater design flexibility and higher design performance.

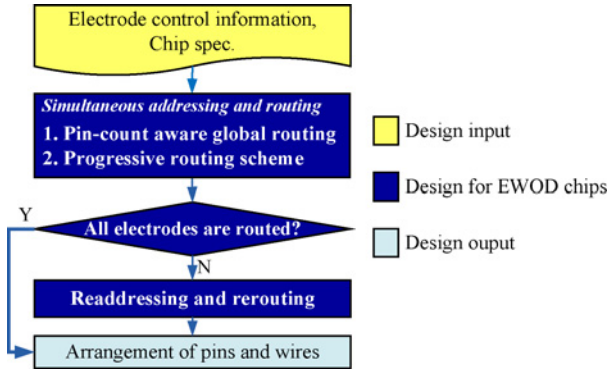


Fig. 3. Our routing algorithm for the EWOD-chip design.

A. Previous Work

To the best knowledge of the authors, there is no previous work in the literature that provides a general pin-count aware routing algorithm for EWOD chips. Most related works focus on pin-constrained electrode-addressing methods [19], [26], [27]. The work by [26] proposes an array-partition based method to group the electrode set without introducing unexpected fluidic-level behaviors. The work by [27] presents a clique-partition based algorithm to formulate compatibility between control signals. By recognizing a minimum clique partition, the required control pins can be optimized. However, since the minimum clique partition is well-known as an NP-hard problem, a heuristic method of iterative clique recognitions is also proposed. The work by [19] further integrates various pin-count saving techniques into fluidic-level synthesis, and then systematically addresses electrodes according to pre-classified categories of pin demand. Although these state-of-the-art works can address the electrodes with fewer and fewer control pins to correctly perform the scheduled fluidic functions, the associated routing problem is still not considered.

B. Our Contributions

In this paper, we propose a novel pin-count aware routing algorithm for broadcast-addressing EWOD chips. Compared with prior design automations, our router is the *first* work in the literature that provides integrated electrode addressing and routing for general chip architectures. Considering both the issues of pin-constrained design and practical routing requirements, our method can simultaneously minimize the required number of control pins and wirelength to achieve better design performance.

As summarized in Fig. 3, we adopt a two-stage technique of pin-count aware global routing followed by a progressive routing scheme to simultaneously consider the electrode addressing and routing problems. Two kinds of flow networks, maximum-flow formulation and minimum-cost maximum-flow formulation, are respectively introduced in each stage to effectively and correctly solve the electrode addressing and routing problems. Besides, a readdressing and rerouting refinement is also proposed to improve the routability. Along with the design flows and algorithms, our contributions include the followings.

1) We propose the *first* design algorithm to deal with the routing problem on broadcast-addressing EWOD chips.

We comprehensively integrate various pin-count saving issues into our two-stage routing technique to reduce the required number of control pins, while keeping the wirelength minimized.

2) In pin-count aware global routing, we derive a maximum-flow formulation with the duality of min-cut property to construct the global routing tracks. By guiding horizontal/vertical routes on these specific tracks, the pin count and wirelength can be simultaneously minimized in a global view.
3) In the progressive routing scheme, we divide the original routing problem into a set of manageable subproblems corresponding to each pin-count expansion. By deriving a minimum-cost maximum-flow network to formulate the pin-count expansion, the required number of control pins can be minimally determined for electrode addressing and routing in each subproblem.
4) In readdressing and rerouting refinement, we introduce a simple yet efficient post refinement to improve the routability. With appropriately and locally handling the unroutable electrodes left from previous routing stages, the entire design overhead can be minimized.

Experimental results demonstrate the scalability and effectiveness of our algorithm. The evaluation performed on a set of real-life chip applications shows that our algorithm achieves the best results in terms of routability, pin-count demand, and wirelength. We also simulate the fluidic-level synthesis and randomly generate several hard test designs to show the robustness of our algorithm.

The remainder of this paper is organized as follows. Section II describes the related preliminaries. Section III points out the design challenge and formally defines the problem and constraints. Section IV details the proposed pin-count aware routing algorithm. Section V analyzes the time complexity of the proposed algorithm. Finally, Sections VI and VII show our experimental results and conclusions.

II. Preliminaries

This section first describes the related background of digital microfluidics and the EWOD chips. Then, the control mechanism of broadcast addressing is detailed.

A. Digital Microfluidics and EWOD Chips

In recent microfluidic technology, liquids have been successfully discretized or *digitized* into independently controllable *droplets* in micro or nano scale. This miniaturization offers several advantages over the traditional continuous-flow or mist-based systems, such as higher sensitivity, lower reagent consumption, and more flexible controls. Moreover, the digitization allows complex microfluidic functions to be efficiently designed via hierarchical and cell-based design methods in modern very large scale integration (VLSI) automation.

In performing various fluidic-handling functions, a primary issue is the manipulation of droplets. Although droplets can be controlled on many driving platforms [12], [18], [23], [25], the EWOD chips, also referred to as EWOD actuators, have received much more attention due to their high accuracy and efficiency, and simple fabrication [13]. The EWOD chip generates electric potential by actuating electrodes to change the wettability of droplets, such that droplets can be shaped and driven along the active electrodes [22], [24], as illustrated in Fig. 4. To induce enough change of wettability for droplet motion, the voltage value applied to electrodes must exceed a threshold. This phenomenon enables a binary bit (i.e., 1/0) to represent a relative logic-high/logic-low value of an actuation voltage, and thus the entire electrode controls can be modeled simply. Furthermore, by patterning electrodes to a general 2-D array and adopting time-varying actuations, many droplet-based operations (e.g., mixing and cutting) can be well-performed on a 2-D array in a *reconfigurable* manner [25].

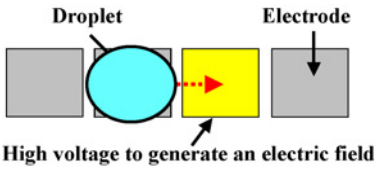


Fig. 4. Droplet control on an EWOD chip.

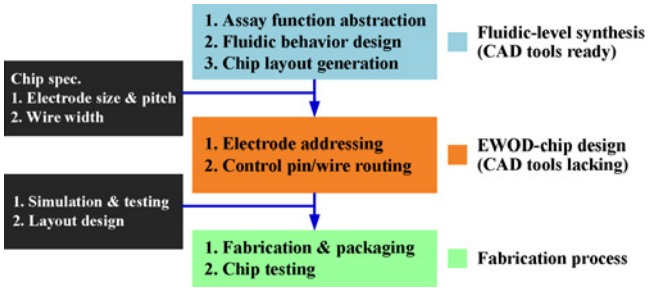


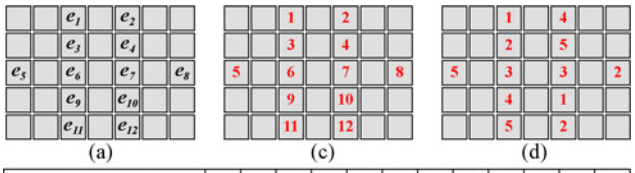
Fig. 5. Regular design flow of a DMF system.

B. Regular Design Flow

A regular design flow of a DMF system can be demonstrated in Fig. 5, which consists of three major stages, fluidic-level synthesis, EWOD-chip design, and fabrication process [15]. Given an assay, the first stage, fluidic-level synthesis, synthesizes a fluidic-behavior outcome as well as a suitable chip layout (i.e., electrode orientation) for performing the given assay. To this end, several computer-aided-design (CAD) tools have been developed for automated designs and optimizations [6], [15], [25]. After the fluidic-level synthesis, controlling information of electrodes for performing synthesized fluidic behaviors can be obtained. In the second stage, EWOD-chip design, electrodes are addressed with control pins to identify the input signals, followed by control-pin routing to establish correspondence between pins and controllers. However, in current literature it appears that no CAD tools are yet available concerning the EWOD-chip routing, which is still inefficiently worked out in manual manner. To resolve this problem, in this paper we shall focus on the automated design of addressing and routing for EWOD chips. When EWOD-chip design is accomplished, the design stage proceeds to fabrication process for chip realization [13], [20].

C. Broadcast Addressing

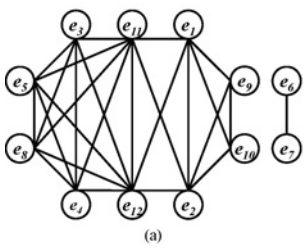
Typically, control signal of moving a droplet in a specific time step can be represented as activated bit "1," deactivated



Electrode	e_1	e_2	e_3	e_4	e_5	e_6	e_7	e_8	e_9	e_{10}	e_{11}	e_{12}
Activation Sequence	1	1	0	0	0	X	X	0	X	X	X	X
	0	0	1	1	1	0	0	1	X	X	X	X
	0	0	0	0	0	1	1	0	0	0	X	X
	X	X	0	0	0	0	0	0	1	1	0	0
	X	X	X	X	1	0	0	1	X	X	1	1

(b)

Fig. 6. (a) Electrodes that are used for handling fluidic functions. (b) Scheduled fluidic functions in the form of activation sequences. (c) Applies the direct-addressing scheme. (d) Applies the broadcast-addressing scheme.



Two electrode grouping results		
Pin	Result 1	Result 2
1	e_1, e_{10}	e_1, e_2
2	e_3, e_8, e_{12}	e_3, e_4, e_8
3	e_6, e_7	e_6, e_7
4	e_2, e_9	e_9, e_{10}
5	e_4, e_5, e_{11}	e_5, e_{11}, e_{12}

(b)

Fig. 7. (a) Compatibility graph G_c derived from Fig. 6(b). (b) Two possible electrode grouping results.

bit "0," or don't care "X." The bit "1"/"0" represents a control signal with a relative logic-high/logic-low value of the actuation voltage. The symbol "X" indicates that the input signal can be either "1" or "0," which has no impact on scheduled fluidic controls [27]. Since droplets are controlled in a time-multiplexed manner, controlling information of electrodes can be obtained by together concatenating these bits and symbols time-step by time-step. The concatenated outcome is called electrode activation sequence. Examples of an electrode set and the corresponding activation sequences are presented in Fig. 6(a) and (b).

To correctly drive these electrodes, control pins must be appropriately assigned to the electrodes for identifying input signals. This approach is also referred to as electrode addressing. Unlike direct addressing, where each electrode is assigned by an independent control pin, broadcast addressing focuses on electrode grouping and control signal merging through the compatibility of activation sequences. Specifically, each electrode activation sequence may contain several don't care terms. By carefully replacing these don't care terms with "1" or "0," multiple activation sequences can be merged to an identical outcome, which is also referred to as the common compatible sequence of these electrodes. Therefore, these electrodes can be assigned by the same control pin to receive the same control signal.

Take electrodes e_4 and e_5 in Fig. 6(b) for example. By replacing "X" in the activation sequence of e_4 with "1," we can merge the activation sequences of e_4 and e_5 to "01001." Therefore, e_4 and e_5 can be addressed with the same control pin due to their mutually compatible activation sequences.

As the example in Fig. 6, (c) and (d), respectively, demonstrate the direct-addressing and broadcast-addressing outcomes. Compared with the direct-addressing result in Fig. 6(c), the broadcast-addressing result in Fig. 6(d) significantly reduces the required control pins from 12 to 5. This reduction requires fewer electrical devices and connections to perform the same fluidic functions, thus improving chip reliability and reducing fabrication cost [27], [28]. Therefore, the derivation of a correct electrode-addressing result under the pin-constrained issue is of great importance, especially in the DMF marketplace.

III. Pin-Constrained Chip Design

This section first points out the difficulties and challenges for pin-constrained chip designs. Then, the practical constraints for broadcast addressing and routing are introduced. Finally, we formulate the design problem for EWOD chips.

A. Design Challenges

Typically, pin-constrained chip design consists of two major stages: 1) broadcast-addressing stage, and 2) routing stage. In the broadcast-addressing stage, the major goal is to correctly address the electrodes with low pin-count demand. To this end, electrode grouping is introduced such that for all electrodes in any group, the corresponding activation sequences are mutually compatible. To specify this manner, a compatibility graph is constructed [27], where the vertex set represents the electrode set and an edge between two electrodes indicates their corresponding activation sequences are compatible. For example, Fig. 7(a) demonstrates a compatibility graph G_c derived from Fig. 6(b). Based on the compatibility graph, the electrode grouping can be mapped to the clique partition problem, which is a well-known example of an intractable problem in graph theory. Since each clique represents an electrode group with mutually compatible control signals, we can individually assign each clique with a dedicated control pin. Accordingly, by recognizing a minimum clique partition in the compatibility graph, the required number of control pins can be optimally minimized. However, the general minimum clique partition is known to be NP-hard [14] and thus is computationally expensive.

After addressing, in the routing stage, wires must be appropriately routed to establish the correspondence between the control pins and the surrounding pads while minimizing the total wirelength. Hence, the routing problem for EWOD chips is similar to the typical escape routing, in which the objective is to individually route all terminal pins to the component (defined as 2-D pin array) boundaries. However, in pin-constrained chip design, multiple electrodes may share the same control pin for pin-count reduction. In other words, a single signal source may contain multi-terminal pins. To realize the electrical connections, multi-terminal pins with the same control signal must first be wired together, and then escape to the component boundaries. This feature makes the typical two-pin-net based escape router unsuitable for the routing problem in EWOD chips. Therefore, a specialized escape routing algorithm must be developed to tackle this problem. Unfortunately, even simply routing for multi-terminal pins with minimum wirelength is also well-known to be NP-complete in most VLSI routing problems [5].

Although a number of heuristics and approximations can separately cope with the two design stages, the potential gap may result in an unsolvable routing problem. As discussed in Section I, separate addressing and routing suffers from an infeasible routing solution, while the simultaneous method provides a higher-quality one (see Fig. 2). The essence of this problem is that the clique partition is not unique and thus multiple electrode grouping results exist. To clarify these points, Fig. 7(b) illustrates the corresponding electrode groups and addressing results of Fig. 2 [result 1 for (a), and result 2 for (b)]. Consequently, to achieve higher design performance, it is necessary to develop an integrated automation for pin-constrained designs. In this regard, the complexity resulting from the multiobjective minimization of pin count and wirelength has become the most difficult design challenge.

B. Broadcast Constraints

As discussed in Section II-C, if a single control pin is assigned to an electrode set, all the corresponding activation sequences of these electrodes must be mutually compatible. Therefore, broadcast constraints (BC) can be formulated as the two following rules.

1) *BC-rule #1:* given an electrode set, if the corresponding activation sequences are mutually compatible, this electrode set can be addressed with the same control pin.
2) *BC-rule #2:* given an electrode set, if the corresponding activation sequences are not mutually compatible, this electrode set cannot be addressed with the same control pin.

C. Routing Constraints

Practically, the wiring connections and media substrate can be formed by using typical integrated circuit (IC) fabrication methods, or existing printed circuit board (PCB) manufacturing processes [3], [13]. In the IC industry, fabrication methods typically rely on thin film planar and photolithography, while the manufacturing processes of PCB are based on electroplating and multilayer lamination [13]. Due to the distinct natures of these technologies, the different wiring criteria involve a variety of routing requirements and constraints. A primary difference is the wiring structures between the two technologies. In PCB-based manufacturing processes, wires can be routed in any angle or even in a rounded manner [1], [2], while the IC-based counterparts restrict most routing to be orthogonal. Thus, without loss of generality, we focus on orthogonal routing such that the horizontal and vertical properties can be realized in both IC-based and PCB-based technologies.

Another significant consideration is the avoidance of electrical defects (e.g., shorts) caused by the shrinkage of wiring clearance. To prevent these faults, the spacing between wires must maintain a threshold; specifically, only a limited number of wires can pass through adjacent pins. Since the capacity between adjacent pins varies with the required electrode size for different bio-applications, it can thus be customized. In this paper, we use the real specification in [13] such that the maximum number of wires between adjacent pins is 3. As in most VLSI routing problems, we focus on uniform grid structure for flexibility and generality.[2] Fig. 8 exemplifies these concerns.

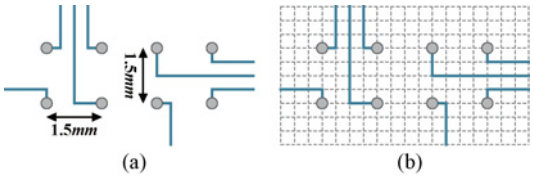


Fig. 8. Number of wires between adjacent pins is 3. (a) Pin array. (b) Grid model.

In addition, a multilayer arrangement of electrical connections necessitates a mechanism for passing signals between layers (e.g., vias and contacts), raising a cost issue in both IC-based or PCB-based fabrication. For example, the cost of PCB prototype fabrication with one, two, four, and six layers is, respectively, U.S.$8.99, U.S.$12.99, U.S.$34.99, and U.S.$59.99, resulting in expenses which increase exponentially with additional layers [1]. Since many biomedical applications prefer disposability, it is likely that using multilayered chips is prohibitively expensive and thus undesirable. Therefore, in this paper, we focus on single-layer routing.

D. Problem Formulation

The pin-constrained design problem for an EWOD chip can be formulated as follows.

Input: *A set E_e of used electrodes for fluidic controls, control information of electrodes in the form of activation sequences, and chip specification.*

Constraint: *Both broadcast constraints and routing constraints should be satisfied.*

Objective: *Derive an electrode-addressing result and establish a routing solution, while minimizing the required control pins and wirelength.*

IV. Algorithm

In this section, we present our pin-count aware routing algorithm. We first discuss the electrode grouping method used in our routing algorithm. Then, the pin-count aware global routing and progressive routing scheme are respectively detailed.

For the purpose of readability and clarity, we use a real-life chip application to exemplify each phase of the proposed algorithm. As illustrated in Fig. 9(a), the chip for DMF based amino acid synthesis contains two types of droplets, functional droplets and wash droplets. The functional droplets (i.e., leucine, phenylalanine, and piperidine droplets) are used for amino acid synthesis, while the wash droplets are used for cleaning contaminations left behind on the surface, to avoid erroneous reaction outcomes. More details can be referred to [21].

A. Electrode Grouping Method

In our pin-count aware routing algorithm, we focus on two kinds of electrode grouping methods in compatibility

[2]Based on the specification, each electrode approximately corresponds to 4 $\times$ 4 grids with respect to the routing grid. Accordingly, an N $\times$ M electrode array corresponds to a 4N $\times$ 4M grid array.

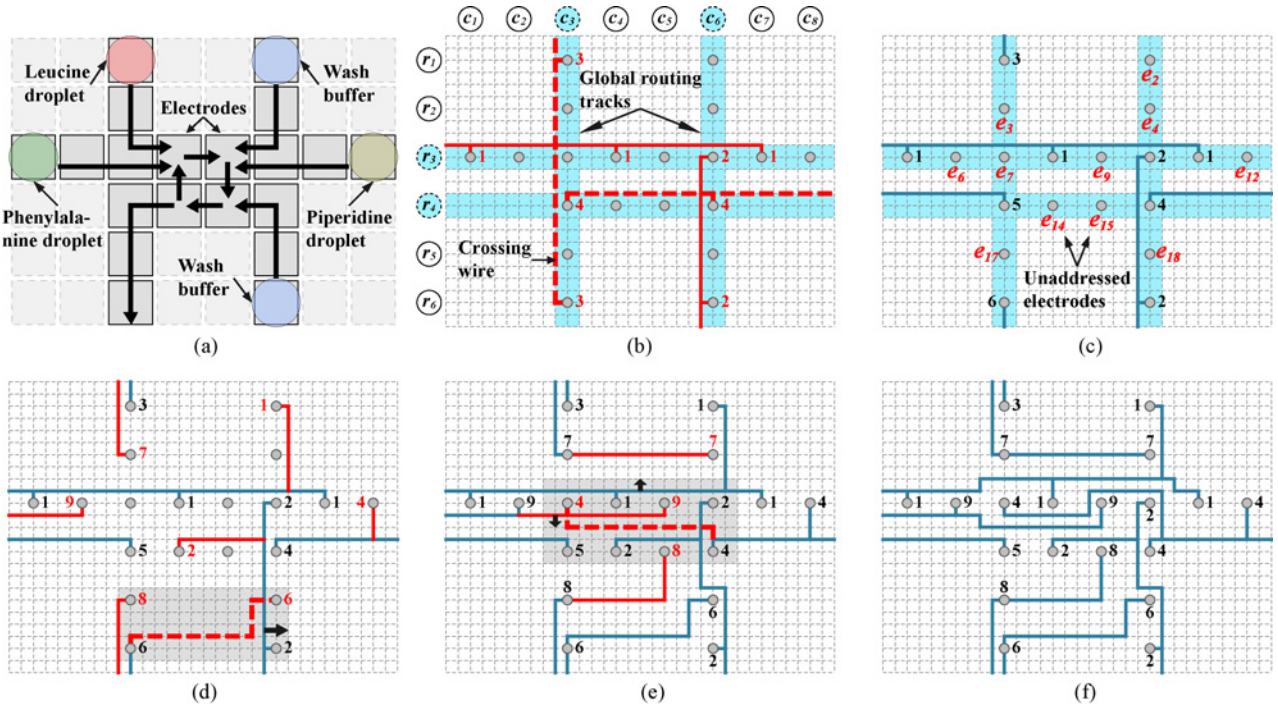


Fig. 9. This real-life chip describes each phase of the proposed pin-count aware routing algorithm. (a) DMF-based amino acid synthesis. (b) Constructs the global routing tracks by maximum-flow (MF) formulation to minimize the pin count. (c) Initial arrangement of control pins and wires after our pin-count aware global routing. (d), (e) Progressive routing scheme with two subproblems. In each subproblem, the electrode addressing and routing are formulated to a minimum-cost maximum-flow (MCMF) network to minimize pin-count expansion. (f) Final arrangement of control pins and wires.

graph G_c, maximum clique and maximum independent set. By recognizing the maximum clique and maximum independent set in G_c, we can identify a maximum electrode group with mutually *compatible* and mutually *incompatible* control signals. Even though general recognitions of maximum clique and maximum independent set are known to be NP-hard, a number of high quality heuristics and approximation algorithms are available in the literature to solve them efficiently. In this paper, we use the heuristic in [17] as our electrode grouping method, which is based on the repeated addition of a candidate vertex with a defined indicator (i.e., vertex degree).

B. Pin-Count Aware Global Routing

The major goal of pin-count aware global routing is to derive an initial arrangement for control pins and wires in a global view, while keeping the pin-count demand and wirelength minimized. To tackle the induced design complexity by simultaneous addressing and routing, we identify the factors that have impact on and attribute to pin-count demand and wirelength as follows.

1) As presented in Fig. 10(a), if the control pins are not carefully assigned to electrodes, the induced routing complexity may trigger more deadlocks or detours between different control pins, implying the orientation of control pins and wires must be well-planned.
2) As presented in Fig. 10(b), if the pins with the same control signal are oriented in a line, a straight wire can connect these pins together without any detour thereby reducing the wirelength.
3) As presented in Fig. 10(c), once the orientation of a wire with a dedicated signal pin is determined, it is desirable to maximize the number of electrodes that can be wired together thereby reducing the pin count and wirelength.

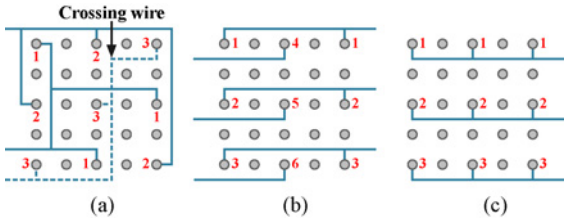


Fig. 10. Factors that impact the pin count and wirelength. (a) Infeasible routing solution. (b) High pin count, longer wirelength. (c) Low pin count, shorter wirelength.

To fully utilize the properties that are favorable for pin-count reduction and wirelength minimization, we construct the global routing tracks on rows and columns in the 2-D pin array, such that all the electrodes can be covered. For each of these global routing tracks (i.e., a certain row or column), we identify a maximum electrode group without signal conflict and assign a dedicated control pin to this group. Then, on this track, conduction wires can be guided on a straight route to this control pin without any detour.

The proposed design technique provides two major advantages: 1) by performing electrode addressing and routing on these global routing tracks, design complexity can be considerably reduced from the whole 2-D pin array to 1-D orientation, and 2) since control pins and wires are well-arranged on these specific tracks in a straight manner, the possibilities of routing detours and deadlocks can be minimized.

1) *Modeling the Global Routing Tracks Construction:* Since each global routing track is assigned by a dedicated

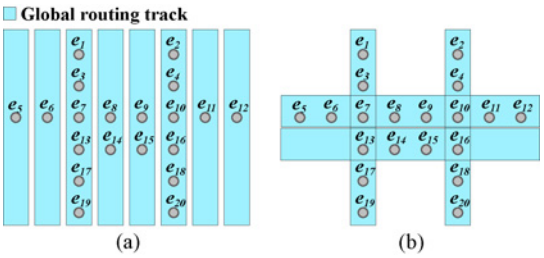


Fig. 11. Two feasible constructions for global routing tracks. (a) Eight tracks (eight columns). (b) Four tracks (two rows and two columns).

control pin, minimizing the pin-count demand requires minimizing the number of global routing tracks. Therefore, the problem for constructing global routing tracks can be formulated as follows.

Given: *A 2-D pin array and an electrode set* E_e.

Objective: *Minimize the number of global routing tracks to cover* E_e.

As the example in Fig. 11, the global routing tracks constructed in Fig. 11(a) require a total of eight tracks (eight columns). Compared with Fig. 11(a), Fig. 11(b) leads to an optimal construction with a total of four tracks (two rows and two columns) to cover all electrodes.

2) *Maximum-Flow Formulation:* To solve the construction problem for global routing tracks, we construct a maximum-flow (MF) graph $G_{mf} = (V_{mf}, E_{mf})$ and propose two formulation rules. The first rule describes the formulation of V_{mf}, and the second rule describes the formulation of E_{mf}. The details of the two MF formulations rules are as follows.

a) *MF-rule #1: formulation of* V_{mf}*:*
   i) For each row i in the 2-D pin array, create a node r_i.
   ii) For each column j in the 2-D pin array, create a node c_j.
   iii) Create a source node s and a sink node t.

b) *MF-rule #2: formulation of* E_{mf}*:*
   i) For each node r_i, create a directed edge $s \rightarrow r_i$ with *one* unit capacity.
   ii) For each electrode $e_k \in E_e$ at row i and column j on the 2-D pin array, create a directed edge $r_i \rightarrow c_j$ with *infinite* capacity.
   iii) For each node c_j, create a directed edge $c_j \rightarrow t$ with *one* unit capacity.

As the example in Fig. 9(b), there is a 2-D pin array with six rows and eight columns, and 20 electrodes used for fluidic controls. By implementing the two formulation rules, the entire flow network G_{mf} can be constructed as illustrated in Fig. 12. Based on the two formulation rules, two theorems can be derived as follows.

Theorem 1: A minimum s-t cut in the flow graph G_{mf}, denoted as $[S, T]$, contains no edge $r_i \rightarrow c_j$.

Proof: Theoretically, an s-t cut of G_{mf} is an edge set $[S, T]$ such that $G_f - [S, T]$ has two components S and T, with $s \in S$ and $t \in T$. According to MF-rule #2, any s-t flow must be the connectivity as $s \rightarrow r_i \rightarrow c_j \rightarrow t$. To disconnect this s-t flow, at least one of the three edges $s \rightarrow r_i$, $r_i \rightarrow c_j$, and $c_j \rightarrow t$ must belong to $[S, T]$. Based on this definition,

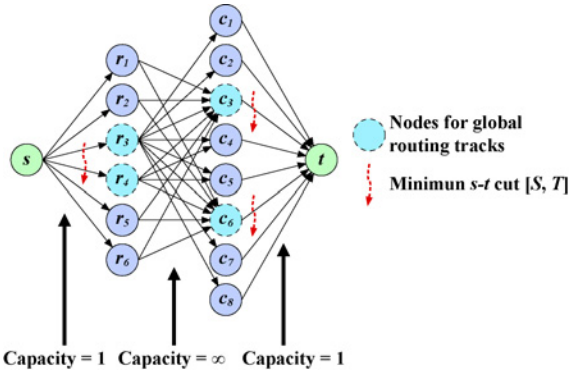


Fig. 12. Example of the maximum-flow based global routing tracks construction for Fig. 9(b).

the minimum s-t cut requires the total of the capacities on the edge set $[S, T]$, denoted as $C[S, T]$, to be minimized. Since the capacity of the edge $r_i \rightarrow c_j$ is assigned as infinite, a minimum s-t cut of G_{mf} consequently contains no edge $r_i \rightarrow c_j$. ■

Theorem 2: The optimal number of global routing tracks is equal to the total of the capacities on the edge set of the minimum s-t cut $[S, T]$ in G_{mf}.

Proof: A feasible solution for global routing tracks requires that all electrodes $e_k \in E_e$ must be covered. According to Theorem 1 and cut property, for each edge $r_i \rightarrow c_j$, at least one of the two ending nodes must belong to the node set of $[S, T]$, denoted as $V_{[S,T]}$. This feature implies that the node set $V_{[S,T]} - \{s, t\}$ covers all the edges $r_i \rightarrow c_j$. In MF-rule #2, each edge $r_i \rightarrow c_j$ represents an used electrode in the 2-D array, meaning that covering all edges $r_i \rightarrow c_j$ is equivalent to covering all electrodes. Referring to MF-rule #1, all the edges $s \rightarrow r_i$ and $c_j \rightarrow t$ are assigned by one unit capacity. And Theorem 1 has shown that $[S, T]$ contains no edge $r_i \rightarrow c_j$. This implies that each cut (i.e., with one unit capacity) in $[S, T]$ can be regarded as one node, r_i or c_j, used to cover the edges $r_i \rightarrow c_j$. Note that the reverse direction that every cover corresponds to a cut is also true as there will be no feasible flow if we remove this cover. Specifically, referring to the property of a cover, it is infeasible to have the connectivity in the form of $s \rightarrow r_i \rightarrow c_j \rightarrow t$ in the resulted flow graph G_{mf} when the cover is removed. Therefore, by deriving a min cut corresponding to a minimum value of $C[S, T]$, we can obtain the minimum number of nodes r_i and c_j to cover all edges $r_i \rightarrow c_j$. In other words, the number of corresponding global routing tracks can be optimally minimized. ■

In duality theorem, a maximum s-t flow value is equal to the minimum capacity of an s-t cut. Therefore, by deriving a maximum flow in G_{mf}, the minimum s-t cut $[S, T]$ can be obtained. Then, based on the two theorems, the global routing tracks can be optimally constructed by tracing the corresponding rows and columns of the node set $V_{[S,T]} - \{s, t\}$, where $V_{[S,T]}$ denotes the node set of $[S, T]$.

As shown in Fig. 12, after deriving a maximum s-t flow, the red-dash arrows represent the edge set of a minimum s-t cut $[S, T]$, and the node set $V_{[S,T]} - \{s, t\}$ is $\{r_3, r_4, c_3, c_6\}$. By tracing the corresponding rows and columns in the 2-D pin array, the global routing tracks can be constructed as illustrated in Fig. 9(b).

3) *Addressing and Routing:* The details of the proposed pin-count aware global routing can be presented in Algorithm 1. We first derive a maximum-flow formulation with the duality of min-cut property to construct the global routing tracks. After the global routing tracks are constructed (lines 2–4), we perform the electrode addressing and routing on these specific tracks such that the design complexity can be greatly reduced from the entire 2-D pin array to these 1-D tracks. As discussed in Fig. 10, for a straight wire on a track it is desirable to connect as many electrodes as possible to minimize the pin-count growth. Accordingly, for each global routing track tk_i, we identify the maximum electrode group without signal conflict, denoted as g_i, by using the proposed technique mentioned in Section IV-A. More specifically, for each track we construct the compatibility graph for those electrodes on the track. Then we identify a maximum clique in the compatibility graph so as to find g_i. Motivated from Fig. 10(c), we prefer to choose a track with the maximum number of electrodes that can be addressed and straightly wired. Obviously, an electrode may be shared with two orthogonal tracks, making cliques derived from different tracks may intersect. This reveals that if electrodes from an identified clique are first addressed and routed, configuration of the other clique intersecting with the identified one may be changed (i.e., size reduction). Certainly, this change will affect the entire topology with respect to the clique size and thus affect our preference on selecting a clique for addressing and routing. For purpose of dynamically updating the topology, a priority queue Q, with the priority of $|g_i|$, is created for storing each tk_i (lines 5–8). Then, we iteratively extract a global routing track tk_i from the priority queue Q, and assign a dedicated control pin to the corresponding g_i (lines 9–11). To minimize the wirelength, a horizontal/vertical wire is guided to route this control pin without any detour (line 12). When crossing a wire, the corresponding electrode group will be decomposed followed by a readdress-and-reroute approach (lines 13–15). After tk_i is processed, the electrode grouping information for each tk_j left in Q is updated (line 16). Finally, iterations end until all global routing tracks are processed (line 17).

We use Fig. 9(b) and (c) to exemplify our pin-count aware global routing. By deriving a MF formulation with the duality of min-cut property, the global routing tracks are constructed on row 3, row 4, column 3, and column 6, as presented in Fig. 9(b). Based on the addressing and routing properties introduced in Fig. 10, we iteratively select a global routing track with the largest non-conflicting electrode group on this track, and assign a dedicated control pin to this group, followed by guiding a horizontal/vertical wire to route these electrodes together, as shown in (b). In case of a crossing point, we identify the smallest electrode group and decompose it for readdressing and rerouting. For example, in (b), the routing for control pin 3 crosses the prerouted wire of control pin 1. Since our router tends to maximize the number of electrodes to share the same control pin, the smaller electrode group on column 3 (pin 3) is thus chosen to be decomposed for readdressing and rerouting. Finally, following pin-count aware global routing, an initial arrangement of control pins and wires can be obtained as illustrated in (c).

Algorithm 1: Pin-Count Aware Global Routing

Input : A 2-D pin array, an electrode set E_e

```
/* tk_i: a global routing track                                  */
/* g_i: the maximum non-conflict electrode group on tk_i        */
/* Q: a priority queue with the priority of |g_i|               */
1  begin
2      construct a maximum-flow network;
3      derive a maximum flow and obtain a minimum cut;
4      construct the global routing tracks;
5      foreach global routing track tk_i do
6          identify g_i on tk_i;
7          Q.PUSH(tk_i);
8      end
9      while Q ≠ φ do
10         tk_i ← EXTRACT-MAX(Q);
11         assign a dedicated control pin to g_i;
12         guide a horizontal/vertical wire to route this control pin;
13         if cross other wires then
14             readdress and reroute;
15         end
16         update g_j of tk_j left in Q;
17     end
18 end
```

Output: Initial arrangement of control pins and wires

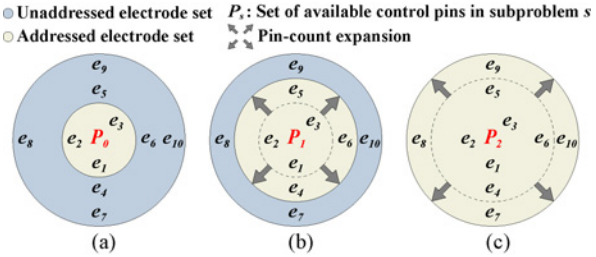


Fig. 13. Basic concept of our progressive routing scheme. (a) Beginning of the progressive routing. (b) Subproblem 1. (c) Subproblem 2.

C. Progressive Routing Scheme

Although the pin-count aware global routing presented in the previous section can derive an electrode addressing and routing result, some electrodes may still not be addressed [see Fig. 9(c)]. Hence, in this routing stage, the major goal is to deal with these unaddressed electrodes left behind, while minimizing the increase of pin count and wirelength.

As modern designs may contain a high number of electrodes, it is computationally costly to handle the routing problem directly. Motivated from [8], we adopt a progressive routing scheme based on the idea of pin-count expansion to solve the routing problem efficiently. The overall concept can be illustrated in Fig. 13. Fig. 13(a) shows the set of existing control pins with an unaddressed electrode set initiated from our global routing. In each subproblem, the entire electrode set is decomposed into two subsets, an unaddressed electrode set and an addressed electrode set. In other words, there are an unaddressed electrode set and an existing pin set for each subproblem. The objective of solving each subproblem is to derive an addressing and routing result while making extra pin-count demand as minimum as possible. More specifically, when solving each subproblem, we intend to maximally utilize the existing control pins for addressing and routing such that the extra pin-count demand can be minimized. After that, the

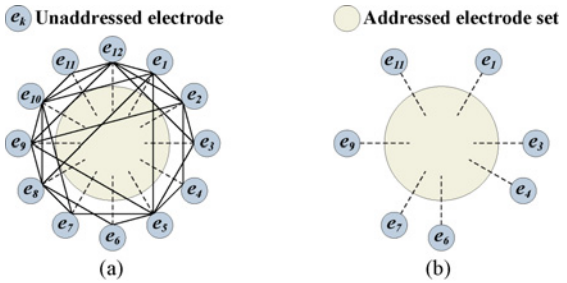


Fig. 14. Motivation of modeling the pin-count expansion. (a) Randomly identifying an electrode group causes a high design complexity. (b) Mutual incompatibility recognition facilitates the problem formulation (i.e., modeling the pin-count expansion) into an efficient one-to-one matching.

pin count is progressively expanded with the addition of extra pin-count demand and the addressing and routing procedures seamlessly proceed to the successive subproblem [see Fig. 13(b), (c)]. The entire procedure ends until all electrodes are addressed and routed [see Fig. 13(c)]. Our progressive routing scheme offers three major advantages as follows.

1) Instead of directly solving the original problem, we focus on each manageably-sized subproblem thereby significantly reducing the entire design complexity.
2) With a strategy of formulating each subproblem into a flow network, the addressing and routing can be efficiently and effectively solved while making the pin-count expansion between successive subproblems minimized.
3) Our progressive routing preserves the previously addressed and routed result between successive subproblems, without numerous modifications such as readdressing and rerouting.

1) *Modeling the Pin-Count Expansion:* The major challenge in our progressive routing scheme is to formulate the problem of pin-count expansion. The essence of pin-count expansion describes the concept of *extra* pin-count demand to realize the electrode addressing and routing for each subproblem s. However, to avoid pin-count overhead, the expansion size must be minimized. Hence, the means by which the set of available control pins in subproblem s, denoted as P_s, can be utilized is the major concern in modeling the pin-count expansion.

The major difficulty in solving each subproblem s is to identify an electrode group from unaddressed electrode set for addressing and routing. As demonstrated in Fig. 14(a), if we randomly identify an electrode group, much of examination of broadcast constraints will be performed for: 1) intra-examination inside the electrode group, and 2) inter-examination between the electrode group and existing pin set. Therefore, this identification method causes high design complexity and thus is hard to be solved efficiently. To tackle this problem, we reverse the regular electrode grouping method. In other words, we identify a maximum unaddressed electrode group, denoted as E'_e, with mutually *incompatible*, rather than compatible, control signals. As demonstrated in Fig. 14(b), this strategy achieves a significant reduction of design complexity, attributed to the removal of intra-examination of constraints inside E'_e. In this manner, the addressing and routing problems can be regarded as a *one-to-one* matching determination between the two sets E'_e and P_s, which greatly facilitates the problem formulation in modeling the pin-count expansion.

After an unaddressed electrode group E'_e is identified, the major goal is to appropriately schedule an electrode addressing and routing result. Since all electrodes $e_k \in E'_e$ must be independently addressed, unaddressed electrodes necessitate extra pin-count demand, implying a pin-count expansion. In order to avoid pin-count overhead, it is desirable to maximize the number of addressed electrodes by utilizing the existing control pins $p \in P_s$ such that the pin-count expansion can be minimized. Furthermore, the associated routing wirelength needs to be minimized. Consequently, for each subproblem s, the problem of pin-count expansion can be formulated as follows.
Given: *A 2-D pin array, P_s, and E'_e.*
Constraint: *Broadcast constraints should be satisfied.*
Objective: *Maximize the number of addressed electrodes by using P_s such that pin-count expansion is minimized, while also minimizing routing wirelength.*

2) *Minimum-Cost Maximum-Flow Formulation:* To minimize pin-count expansion, we construct a minimum-cost maximum-flow (MCMF) graph $G_{\text{mcmf}} = (V_{\text{mcmf}}, E_{\text{mcmf}})$ and propose two formulation rules. The first rule describes the formulation of V_{mcmf}, and the second rule describes the formulation of E_{mcmf}.

The key idea behind our MCMF formulation is to map the objective "maximize the number of addressed electrodes by using P_s" into "maximum flow value" in G_{mcmf}, with "minimize the routing wirelength" corresponding to "minimum flow cost." To avoid any violation of broadcast constraints in our MCMF formulation, we define the control pin set $P_s^k \in P_s$ for each electrode $e_k \in E'_e$ such that e_k can be addressed with the control pin $p \in P_s^k$. By identifying the compatibility between e_k and those addressed electrodes with control pins $p \in P_s$, the P_s^k can be obtained. Since the wirelength for routing an electrode e_k with the control pin $p \in P_s^k$ should be minimized, we define the routing cost as follows:

$$Cost(e_k, p) = \sum(\alpha \cdot g_c + \beta \cdot g_n), \forall e_k \in E'_e, p \in P_s^k \qquad (1)$$

where $Cost(e_k, p)$ represents the pin-to-wire routing cost from electrode $e_k \in E'_e$ to the routed wire of control pin $p \in P_s^k$. Since our routing is based on uniform grid structure, if the routing for e_k crosses another wire in the grid point g_c, a high penalty α is assigned; otherwise a low cost β is assigned to the non-crossing grid point g_n. Then, we perform the A* maze searching method to find a minimum cost routing path. In this paper, we empirically set $\alpha = 10$ and $\beta = 0.1$.

The two MCMF formulations rules can be detailed as follows.

a) *MCMF-rule #1: formulation of V_{mcmf}.*
   i) For each electrode $e_k \in E'_e$, create a node v_{e_k}.
   ii) For each control pin $p \in P_s$, create a node v_p.
   iii) Create a source node s', and a sink node t'.

b) *MCMF-rule #2: formulation of E_{mcmf}.*
   i) For each node v_{e_k}, create a directed edge $s' \rightarrow v_{e_k}$ with *one* unit capacity and *zero* cost per unit flow.
   ii) For each node pair (v_{e_k}, v_p), where $e_k \in E'_e$ and

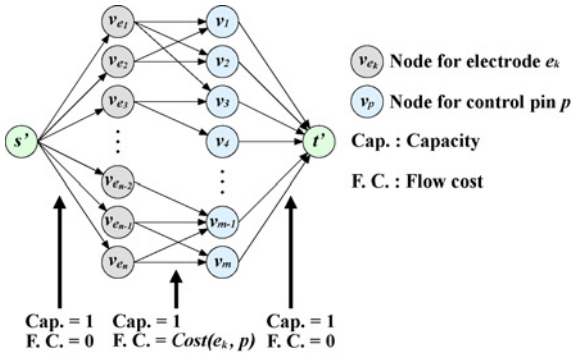


Fig. 15. Formulates pin-count expansion to the minimum-cost maximum-flow network.

$p \in P_s^k$, create a directed edge $v_{e_k} \rightarrow v_p$ with *one* unit capacity and $Cost(e_k, p)$ cost per unit flow.

iii) For each node v_p, create a directed edge $v_p \rightarrow t'$ with *one* unit capacity and *zero* cost per unit flow.

Fig. 15 shows a general diagram of the MCMF formulation. Based on the proposed MCMF formulation rules, we have the following two theorems.

Theorem 3: A feasible $s' - t'$ flow represents a correct electrode addressing without any violation of broadcast constraints.

Proof: Based on the constructed MCMF network, a feasible flow f must be the connectivity as $s' \rightarrow v_{e_k} \rightarrow v_p \rightarrow t'$. Since all the edge capacities in our MCMF formulation are set to be one, the flow value of f must be one and thus can be regarded as addressing electrode e_k with control pin p. According to the MCMF-rule #2, for each electrode e_k, the edge $v_{e_k} \rightarrow v_p$ is constructed only for control pin $p \in P_s^k$. As the definition, P_s^k is obtained by tracing all the existing control pins that can be assigned to e_k. Therefore, edge connections between v_{e_k} and v_p comply with broadcast constraints. Moreover, the capacity assignment restricts each control pin can be only assigned to one electrodes, guaranteeing a correctness that no multiple electrodes share the same control pin as they are mutually-incompatible. As a consequence, for any feasible flow in the connectivity as $s' \rightarrow v_{e_k} \rightarrow v_p \rightarrow t'$, it represents an valid and correct addressing result by addressing electrode e_k with control pin p. ■

Theorem 4: Based on the proposed MCMF network, we can adopt the MCMF algorithm to optimally maximize the number of addressed electrodes with minimum total routing costs.

Proof: Theoretically, the MCMF problem is to find a set of feasible flows, with minimum total cost. According to Theorem 3, any feasible flow represents a correct electrode addressing, and thus the number of addressed electrodes is equal to the total flow value. In addition, the flow cost in our MCMF network is modeled as the defined routing cost, as formulated in MCMF-rule #2. Therefore, by adopting the MCMF algorithm, the number of addressed electrodes can be optimally maximized with minimum total routing costs. ■

Based on the two theorems, we can maximize the number of addressed electrodes by deriving a maximum flow value in G_{mcmf} and have the following lemma.

Lemma 1: The extra pin-count demand for electrode addressing is equal to $|E'_e| - f_{\text{mcmf}}$, where f_{mcmf} denotes the maximum flow value in G_{mcmf}.

Proof: Since the maximum flow value f_{mcmf} represents the maximum number of addressed electrodes, the number of unaddressed electrodes is equal to $|E'_e| - f_{\text{mcmf}}$. As discussed, each of these unaddressed electrodes necessitates dedicated control pins due to their mutually incompatibility. To correctly address these electrodes, the extra pin-count demand for electrode addressing is equal to $|E'_e| - f_{\text{mcmf}}$. ■

3) *Addressing and Routing:* The details of the proposed progressive routing scheme can be presented in Algorithm 2. As discussed before, our progressive routing scheme divides the original problem into a set of manageable subproblems corresponding to each pin-count expansion. In the beginning of each subproblem s, we first identify and select the electrode group E'_e from unaddressed electrodes (lines 2, 3). In other words, we construct the compatibility graph from unaddressed electrodes and identify a maximum independent set. Then, electrode addressing and routing are well-formulated into an MCMF network for maximum utilization of the existing control pins. By deriving a maximum flow value with minimum cost, pin-count expansion can be minimized while maintaining low routing costs (lines 4, 5). Since the solution of the MCMF network represents a solution of electrode addressing and routing, by tracing the MCMF network we can obtain an addressing and routing result (lines 6, 7). According to Lemma 1, if $|E'_e|$ is larger than the flow value f_{mcmf}, extra pin count must be included, implying a pin-count expansion. That is, these electrodes must be independently addressed with dedicated control pins and directly routed to the boundary (lines 8–13). After all electrodes $e_k \in E'_e$ are addressed and routed, the potential existence of crossing wires must be removed. To avoid runtime overhead caused by numerous modifications of current results, a local rerouting approach (explained later in this section) without extra pin-count demand is introduced to handle this problem (lines 14–17). Iterations of subproblems end until all electrodes are addressed (line 18).

We use Fig. 9(c)–(f) to clarify our progressive routing scheme. After pin-count aware global routing, an initial arrangement of control pins and wires can be shown in Fig. 9(c). The set of existing control pins in Fig. 9(c), $P_1 = \{1, 2, 3, 4, 5, 6\}$, is the input pins of the first subproblem in the progressive routing scheme. Then we identify a maximum electrode group with mutually incompatible control signals, $E'_e = \{e_2, e_3, e_6, e_{12}, e_{14}, e_{17}, e_{18}\}$, from unaddressed electrode set. In the first subproblem, the goal is to utilize the set of existing control pins, $P_1 = \{1, 2, 3, 4, 5, 6\}$, for addressing and routing the electrode group E'_e thereby minimizing the pin-count expansion. By formulating this issue into the MCMF network, a maximum addressing with minimum routing costs can be derived as shown in Fig. 9(d). In more detail, electrodes $\{e_2, e_{12}, e_{14}, e_{18}\}$ are respectively addressed using existing control pins $\{1, 4, 2, 6\}$; while the electrodes $\{e_3, e_{17}, e_6\}$ are directly addressed with independent control pins $\{7, 8, 9\}$, implying a pin-count expansion with size 3. Since the routing cost in our MCMF network is estimated by minimum crossing points and wirelength, some wires may cross prerouted wires.

Algorithm 2: Progressive routing scheme

Input : Initial addressing and routing result from global routing

```
/* s: subproblem s ← 0                                   */
/* f_mcmf: maximum flow value of G_mcmf                  */
1  begin
2    while existing an unaddressed electrode do
       // begin of subproblem s ← s + 1
3      identify the electrode group E'_e;
4      construct the MCMF network;
5      solve the MCMF network to minimize the pin-count
       expansion;
6      trace the addressing and routing from MCMF network;
7      update the arrangement of control pins and wires;
8      if |E'_e| − f_mcmf > 0 then
         // pin-count expansion
9        foreach unaddressed electrode e'_k ∈ E'_e do
10         address e'_k with dedicated control pin;
11         route this pin to boundary;
12       end
13     end
14     while existing a crossing wire do
15       identify a rerouting region;
16       reroute;
17     end
       // end of subproblem s
18   end
19 end
```

Output: Arrangement of control pins and wires

Algorithm 3: Readdressing and Rerouting Refinement

Input : An infeasible routing solution with unroutable electrodes

```
/* tk_i: a global routing track                          */
/* e_k: an unroutable electrode                          */
/* e'_k: a neighboring prerouted electrode of e_k        */
1  begin
2    foreach global routing track tk_i do
3      foreach unroutable electrode e_k on tk_i do
4        select neighboring prerouted electrodes e'_k of e_k;
5        if e_k is routable by readdressing and rerouting e'_k then
6          readdressing and reroute e_k and e'_k;
7        end
8      end
9    end
10 end
```

Output: Arrangement of control pins and wires

For example, in Fig. 9(d), the red-dash wire for control pin 6 cannot be routed as it is blocked by the prerouted wire of control pin 2. For this crossing wire, we identify the encompassed bounding box enlarged by b unit as the rerouting region [see the shadow area in Fig. 9(d)]. Empirically, b is initialized by 1 and will incrementally increase by one unit until it is routed successfully. Then, we iteratively choose a wire from the outer to the inner region, and route this wire along the outer region as much as possible to free more routing resources for inner wires. As the example in Fig. 9(d), the prerouted wire of control pin 2 will be rerouted along the outer region such that the crossing problem can be resolved.

After all electrodes $e_k \in E'_e$ are addressed and routed in the first subproblem, the pin count is progressively expanded by a minimal requirement (from 6 to 9). Then, our routing procedure seamlessly proceeds to the successive subproblem initiated by the previous arrangement of control pins and wires. By adopting the same subroutine [see Fig. 9(e)], the solution of control pins and wires can eventually be obtained as shown in Fig. 9(f).

D. Readdressing and Rerouting Refinement

As our algorithm comprehensively integrates pin-count savings issues into the routing, it may potentially create detour and congestion problems between wiring multiple control pins together. For some EWOD chips with high-density electrodes (i.e., hundreds of electrodes), such problems may become even critical and potentially lead to an infeasible routing solution. To make the design more feasible, we introduce a readdressing and rerouting refinement to deal with this issue. The proposed readdressing and rerouting scheme conducts a post refinement to an infeasible routing solution. An EWOD-chip design with infeasible routing solution has some unroutable electrodes after we adopt the pin-count aware global routing and progressive routing. In broadcast addressing, since a wire may connect multiple electrodes to share the same control signal, some electrodes may be blocked once the number of wires increases. Therefore, the major idea behind the proposed refinement is trying to reroute those prerouted electrodes by readdressing them with *extra/dedicated* control pins to create more routing regions and paths for unroutable electrodes.

Fig. 16 gives an illustration of the readdressing and rerouting refinement. In Fig. 16(a), there is one electrode which cannot be successfully routed because wiring pin 6 and pin 5 has blocked the routing region of this electrode. In the readdressing and rerouting refinement, we try to select its neighboring electrodes and then readdressing and rerouting them by assigning dedicated control pins. As in Fig. 16(b), the original two electrodes with pin 6 are decomposed into two separate groups of pin 6 and pin 7 such that the blocking situation can be removed. Hence, the unroutable electrode in Fig. 16(a) can now be readdressed by a new pin 8 and successfully routed.

As many post-refinement techniques in VLSI routing (e.g., rip-up and reroute), a means to identify a refinement region locally is an important consideration. The reason is that we want to preserve the previously arranged addressing and routing solution without too much post modification which always incurs design overhead. Referring to our network-flow based algorithm, the global routing first constructs a set of global routing tracks with minimum cardinality. Then, the progressive routing iteratively completes the addressing and routing on these tracks. In other words, the entire routing solution maintains an arrangement orderly expanded from the constructed global routing tracks. This feature reveals an efficient refinement procedure based on these global routing tracks.

Regarding these concerns, the proposed readdressing and rerouting refinement can be presented in Algorithm 3. First, we iteratively identify a global routing track tk_i (line 2). For each unroutable electrode e_k on the track tk_i, we select the neighboring prerouted electrodes e'_k of e_k and try to readdressing and reroute e'_k by a dedicated control pin. Then, we check the feasibility of such a readdressing and rerouting refinement and allow it once e_k can be readdressed and rerouted successfully (lines 3–8).

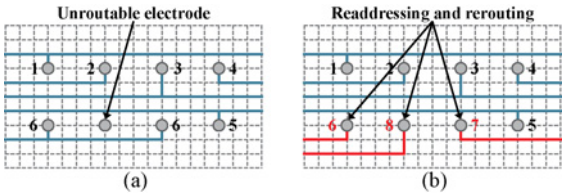


Fig. 16. (a) EWOD-chip design with one unroutable electrode. (b) Readdressing and rerouting refinement.

V. Time Complexity Analysis

The runtime bottleneck of our algorithm comes from the two network-flow based routing stages, pin-count aware global routing and progressive routing. Let E_e denote the electrode set. In the MF formulation of global routing stage, the sizes of node set V_{mf} and edge set E_{mf} are $O(|E_e|)$ by referring to the two formulation rules, MF-rule #1 and MF-rule #2. Hence, the global routing problem can be solved in $O(|E_e|^2 log(|E_e|))$ time complexity by implementing the blocking flow algorithm in [10]. In the MCMF formulation of progressive routing stage, the sizes of node set V_{mcmf} and edge set E_{mcmf} are also $O(|E_e|)$ by referring to the two formulation rules, MCMF-rule #1 and MCMF-rule #2. In solving each MCMF formulation, the time complexity can be $O(|E_e|^3)$ by implementing the MCMF algorithm in [7]. Then, since there are totally at most $|E_e|$ progressive iterations, the progressive routing stage can be completed in $O(|E_e|^4)$.

Theorem 5: Given an electrode set E_e, the routing problem of EWOD chips can be solved in $O(|E_e|^3)$ time complexity by the proposed algorithm.

Proof: Based on the previous analysis, the naive examination of time complexity is $O(|E_e|^4)$, which is bounded by the progressive routing stage. To be more accurate, the progressive routing stage decomposes the electrode set into several electrode subsets corresponding to each MCMF-network subproblem. Suppose each electrode subset is denoted as E_e^i, then the time complexity of the progressive routing can be rewritten as $O(\Sigma|E_e^i|^3)$. By multinomial theorem [9], the term $\Sigma|E_e^i|^3$ is always less than $(\Sigma|E_e^i|)^3$. Since in our progressive routing procedure the electrode subsets are decomposed in a disjoint manner, thus we have $\Sigma|E_e^i| = |E_e|$. Consequently, we have a more exact time complexity as $O(|E_e|^3)$. ■

VI. Experimental Results

We implement the proposed algorithm in C++ language on a 2 GHz 64 bit Linux machine with 16 GB memory. We evaluate our routing algorithm on a set of real-life chip applications [21], [25], [27] for amino-acid synthesis, protein synthesis, protein dilution, multiplexed assay, and multi-functional chip, as listed in Table I. To demonstrate our robustness, we simulate the fluidic-level synthesis in larger scale (e.g., at most 30 droplets and 150 electrodes) and randomly generate seven hard test chips, as listed in Table I. For comparison purpose, we implement the direct addressing with maze routing, denoted as DA-maze, to independently route each electrode to component (2-D pin array) boundary. To further show the performance of our integrated routing algorithm, we separately implement the broadcast addressing and routing, denoted as BA-maze. In BA-maze, we use the heuristic in [27] as the broadcast-addressing manner. As discussed in Section III-A, the routing problem for a broadcast-addressing result is an NP problem (multi-terminal pins routing). Therefore, we use a heuristic based on maze routing to sequentially and iteratively route a nearest electrode pair with the same control pin until all electrodes are routed. Note that in this paper we measure the wirelength by computing the number of grids through which wires pass (i.e., a pair of adjacent grid points corresponds to one unit wirelength).

Table I lists the overall comparison results. First, our algorithm shows better routability by completing all 14 test cases (100.0%), while the DA-maze and the BA-maze complete only 7 (50.0%) and 8 (57.1%) test cases, respectively. We observe that there is only one case of multi-function cannot be successfully routed by the major two network-flow based routing stages (i.e., pin-count aware global routing and progressive routing scheme). Detailed failure data are: #Pin = 41, WL = 1581, #Fail = 8, and CPU = 1.01. Though, after conducting the proposed readdressing and rerouting refinement, the routability problem in this case can be removed (i.e., #Fail = 0). As a whole, these results demonstrate that our algorithm yields stronger effectiveness in terms of pin count, wirelength, and routability on both real-life and hard test chips.

Since the number of failed designs is different, it is hard to fairly perform a direct comparison between the two methods and ours in terms of pin count, wirelength, and runtime. Therefore, we focus on these chips which are completed by both our method and another approach as listed in Tables II and III. In the first comparison with DA-maze, Table II shows that our algorithm achieves 62.8% pin-count reduction and produces 25.5% shorter wirelength, with the reasonable CPU time. Compared with direct addressing, this result shows that the broadcast addressing requires only a small number of control pins to perform the same fluidic functions. Moreover, without complicated wiring connections, the system reliability and fabrication process can be significantly improved. Note that in the three cases, amino-acid-1, amino-acid-2, and random-2, the wirelength obtained by our algorithm is slightly longer than that of DA-maze. The reason is that many electrodes in these three cases locate nearly at the outermost chip region such that they can be directly routed to the chip boundary in shorter wirelength. However, since the proposed algorithm focuses on broadcast addressing that minimizes the pin count by routing multiple electrodes together, some extra wirelength may potentially be demanded.

In the second comparison, we compare our integrated method with BA-maze which is based on separate broadcast addressing and routing, respectively in terms of pin count, wirelength, and runtime. As listed in Table III, we reduce the pin count by 14.2%, and shorten the wirelength by 34.1% with small increase of CPU time. By simultaneously considering the pin-count reduction and wirelength minimization, our method can effectively achieve greater design performance and higher-level integration.

A. Routability Estimation

We conduct an experiment to evaluate the relationship between the routability and electrode density. The routability is

TABLE I
COMPARISON BETWEEN THE DA-MAZE, THE BA-MAZE, AND OUR ALGORITHM

Chip	Size	#E	Direct Addressing				Broadcast Addressing							
			DA-Maze				BA-Maze				Ours			
			#Pin	WL (#Grid)	#Fail	CPU time (s)	#Pin	WL (#Grid)	#Fail	CPU time (s)	#Pin	WL (#Grid)	#Fail	CPU time (s)
Amino-acid-1	6 × 8	20	20	156	0	0.02	13	254	0	0.03	9	190	0	0.08
Amino-acid-2	8 × 8	24	24	168	0	0.04	16	236	0	0.05	11	207	0	0.11
Protein-1	13 × 13	34	–	–	1	–	19	814	0	0.43	24	462	0	0.26
Protein-2	13 × 13	51	–	–	3	–	21	898	0	0.16	25	662	0	0.28
Dilution	15 × 15	54	–	–	1	–	–	–	7	–	15	1178	0	0.17
Multiplex	15 × 15	59	–	–	1	–	–	–	7	–	36	1444	0	0.36
Multi-function	15 × 15	81	–	–	7	–	–	–	11	–	56	1911	0	1.44
Random-1	10 × 10	20	20	281	0	0.01	14	353	0	0.02	8	278	0	0.04
Random-2	15 × 15	30	30	560	0	0.04	18	1053	0	0.05	11	614	0	0.10
Random-3	20 × 20	60	–	–	1	–	23	4678	0	0.18	19	2720	0	0.31
Random-4	30 × 30	90	90	8924	0	0.33	31	8558	0	0.37	26	5975	0	0.48
Random-5	50 × 50	100	100	10 945	0	1.19	–	–	23	–	37	7965	0	1.53
Random-6	60 × 60	100	100	11 344	0	1.48	–	–	27	–	41	8901	0	2.23
Random-7	70 × 70	150	–	–	22	–	–	–	31	–	80	16 612	0	6.65
Total					36				106				0	

#E: number of used electrodes for fluidic controls. #Pin: number of used control pins for electrode addressing.
#Fail: number of failed electrodes (unable to find a valid addressing and routing manner).
WL: total wirelength computed by the number of routing grids.

TABLE II
COMPARISON BETWEEN THE DA-MAZE AND OUR ALGORITHM

Chip	DA-Maze			Ours		
	#Pin	WL (#Grid)	CPU Time (s)	#Pin	WL (#Grid)	CPU Time (s)
Amino-acid-1	20	156	0.02	9	190	0.08
Amino-acid-2	24	168	0.04	11	207	0.11
Random-1	20	281	0.01	8	278	0.04
Random-2	30	560	0.04	11	614	0.10
Random-4	90	8924	0.33	26	5975	0.48
Random-5	100	10 945	1.19	37	7965	1.53
Random-6	100	11 344	1.48	41	8901	2.23
Total	384	32 378	3.11	143	24 130	4.57

TABLE III
COMPARISON BETWEEN THE BA-MAZE AND OUR ALGORITHM

Chip	BA-Maze			Ours		
	#Pin	WL (#Grid)	CPU Time (s)	#Pin	WL (#Grid)	CPU Time (s)
Amino-acid-1	13	254	0.03	9	190	0.08
Amino-acid-2	16	236	0.05	11	207	0.11
Protein-1	19	814	0.43	24	462	0.26
Protein-2	21	898	0.16	25	662	0.28
Random-1	14	353	0.02	8	278	0.04
Random-2	18	1053	0.05	11	614	0.10
Random-3	23	4678	0.18	19	2720	0.31
Random-4	31	8558	0.37	26	5975	0.48
Total	155	16 844	1.29	133	11 108	1.66

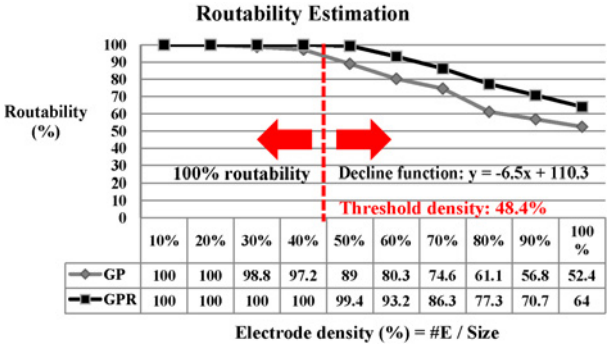


Fig. 17. Relationship between routability and electrode density.

defined as the success rate of addressed and routed electrodes. The electrode density is defined as the ratio between $\#E$ (i.e., the number of used electrodes for fluidic controls) and the chip size. Evaluation is performed on a 50 × 50 array which is large enough to accommodate all existing designs in the literature. We randomly generate cases for different electrode densities ranged from 0% to 100%. In order to see the benefit from the proposed refinement (i.e., readdressing and rerouting), we evaluate the routability of our routing algorithm with and without the refinement, which are respectively denoted as GP (i.e., global routing + progressing routing) and GPR (i.e., global routing + progressing routing + refinement).

As depicted in Fig. 17, the routability is plotted as a function of electrode density. We see that the proposed refinement does not work until the electrode density grows to nearly 30.0%, at which GP begins with some unroutable electrodes. Regarding the electrode density from 30.0% to 100.0%, the proposed refinement improves the routability by maximally 16.2% and averagely 10.1%. On the other hand, we observe that the entire routing procedure, GPR, achieves 100% routability by reaching a threshold density 48.4%, and then declines linearly with respect to the growth of electrode density (i.e., approximately it has a decline function $y = -6.5x + 110.3$). As reported in [6], [11], and [20], currently developed chips mostly have the electrode density around 10%∼35%. There are two major causes: 1) different applications target on different electrode orientations to optimize the fluidic performance, thus making only a part of cells on the 2-D array be manufactured to electrodes, and 2) on-chip modules such as magnets and

electrophoresis devices are embedded on the array for applications such as DNA purification and sample preparation; these modules are independent from EWOD-based controls whereas they still occupy a part of the space on the 2-D array. For example, a recently developed large-scale chip of n-plex immunoassay, embedded nearly 1200 electrodes and several on-chip magnet modules on a 51×76 array, has the electrode density about 31.0% [4]. Consequently, considering the above discussions and experimental results, our router is scalable enough and capable of handling currently developed chips.

VII. Conclusion

In this paper, we proposed the *first* pin-count aware routing algorithm to deal with the routing problem on broadcast-addressing EWOD chips. Based on two kinds of flow formulations, maximum-flow network and minimum-cost maximum-flow network, as well as an appropriate readdressing and rerouting refinement, the electrode addressing and routing problems can be correctly and effectively solved. By comprehensively integrating various pin-count saving issues into our routing steps, our router can lead to a superior addressing and routing solution with lower pin count, higher routability, and shorter wirelength to realize low-cost and reliable microfluidic actuators. Experimental results on real-life chip applications and hard test designs have demonstrated the robustness, effectiveness, and scalability of our algorithm.

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