Chip-Level Design and Optimization for Digital Microfluidic Biochips

Tsung-Wei Huang*, Yan-You Lin†, Jia-Wen Chang*, Tsung-Yi Ho*,
*Department of Computer Science and Information Engineering, National Cheng Kung University, Tainan, Taiwan
†Department of Electrical and Computer Engineering, Duke University, Durham, NC

***Abstract*—Recently, digital microfluidic biochips (DMFBs) have revolutionized many biochemical laboratory procedures and received much attention due to their advantages such as high throughput, automatic control, and low cost. To meet the challenges of increasing design complexity, computer-aided-design (CAD) tools have been involved to build DMFBs efficiently, where a two-stage design flow of fluidic-level synthesis followed by chip-level design are generally applied. Regarding fluidic-level synthesis, many related studies and CAD tools have been well-developed to synthesize the fluidic behaviors efficiently and effectively. However, research findings being highly-concerned with the chip-level design are still critically lacking. In this paper, we shall focus on chip-level design and discuss related background and two major optimization problems posed by electrode addressing and control pin routing. We show how CAD tools are involved to automate and optimize the two design problems. With this assistance, users can concentrate on the development and abstraction of nanoscale bioassays while leaving chip optimization and implementation details to CAD tools.**

I. Introduction

Recently, *droplet*-based digital microfluidic biochips (DMFBs), have emerged as a popular alternative for laboratory experiments. By controlling miniaturized and discrete liquids (i.e., droplets), DMFBs offer various advantages including high portability, high throughput, high sensitivity, less human intervention, and low sample volume consumption. Due to these advantages, practical applications such as clinical diagnostics, DNA analysis, environmental toxin monitoring, point-of-care testing, and drug discovery have been successfully realized on DMFBs [10], [22].

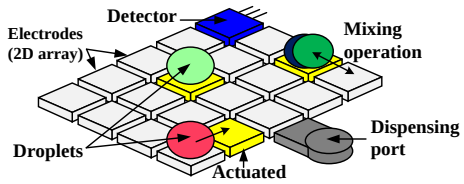


Figure 1. The schematic view of a DMFB.

Generally, a DMFB consists of a two-dimensional (2D) electrode array and peripheral devices (e.g., optical detector, dispensing port, etc.), as schematically shown in Figure 1 [22]. On a DMFB, the sample carriers, *droplets*, are controlled by underlying electrodes using electrical actuations to generate electrowetting force (i.e., a principle called electrowetting-on-dielectric or EWOD) [17]. By assigning time-varying voltage values to turn on/off electrodes, droplets can be moved around the entire 2D array to perform fundamental operations (e.g., dispensing and mixing). These operations are carried out under clock control in a *reconfigurable* manner due to their flexibility in spatial and time domain [4].

As the use of DMFBs increases, their complexity is expected to become significant due to the need for multiple and concurrent assay functionality on the chip, as well as more sophisticated control for resource management. Hence, conventional full-custom design techniques will not scale well for larger designs [10], [22]. Considering an efficient development of DMFBs, there is a pressing need to deliver the same level of computer-aided-design (CAD) tools to DMFB users and designers that the semiconductor industry takes for granted. Design automation approaches are expected to relieve the design burden of manual optimization of assays, time-consuming chip designs, and costly testing and maintenance procedures. Besides, CAD tools will facilitate the integration of fluidic components with a microelectronic component in next-generation system-on-chips (SOCs).

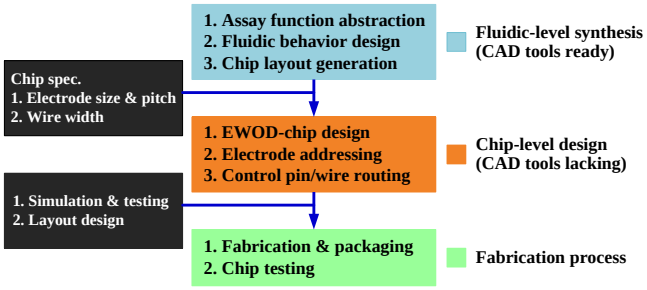


Figure 2. Regular design flow of a DMFB.

A regular design flow of a DMFB is demonstrated in Figure 2, which consists of three major stages, fluidic-level synthesis, chip-level design, and fabrication process [10]. First, the DMFB users provide the fluidic protocol for nano- or micro-scale assay. The first stage, fluidic-level synthesis, synthesizes a fluidic-behavior outcome as well as a suitable chip layout (i.e., electrode orientation) for performing the given assay. To this end, several high-quality CAD tools have been developed for automated designs and optimizations of fluidic performance [10], [11], [15], [20], [21], [22], [27].

After the fluidic-level synthesis, controlling information of electrodes for performing synthesized fluidic behaviors can be obtained. In the second stage, chip-level design, electrical connections are planned to establish signal transmission for correct controls of fluidic behaviors. As DMFBs typically rely on electrowetting-on-dielectric (EWOD) based actuator, called EWOD chip or EWOD actuator, this design stage is also referred to as EWOD-chip design [17]. In this design stage, electrodes are addressed with control pins to identify the input signals, followed by wire routing to establish correspondence between pins and controllers. Chip-level design is a key consideration as it dominates the solution quality of electrical connections and signal plan, which is directly related to manufacturing complexity and fabrication cost [1], [8], [10]. However, readily available CAD tools concerning the chip-level design are still critically lacking. Most design efforts devoted to devising EWOD chips are worked out manually, which might suffer from either poor solution quality or time-consuming human effort.

In this paper, we present an overview of an automated chip-level design for DMFBs that addresses the derivation of electrode addressing and wire routing on EWOD chips. We provide a survey of key CAD approaches that are developed recently and discuss

978-1-61284-857-0/11/$26.00 ©2011 IEEE

related background to give a holistic perspective on the chip-level design. With these CAD approaches, DMFB designers and users can concentrate on the development of the nano and microscale bioassays, leaving chip optimization details (i.e., signal plan and electrical connections in particular) to the CAD tools.

Organization of the remainder of the paper is as follows: Section II reviews the technology and architecture of the EWOD chip. Section III and Section IV discuss the two major design steps of electrode addressing and wire routing in the chip-level design, respectively. Section V describes the design challenges and several open problems that remain to be tackled. Finally, conclusion is drawn in Section VI.

II. Architecture and Design Model of EWOD Chips

In performing various fluidic-handling functions, a primary issue is the manipulation of droplets. Although droplets can be controlled on many driving platforms [22], the EWOD chips, also referred to as EWOD actuators, have received much more attention due to their high accuracy and efficiency, and simple fabrication [8]. The EWOD chip generates electric potential by actuating electrodes to change the wettability of droplets, such that droplets can be shaped and driven along the active electrodes [17], [19]. To induce enough change of wettability for droplet motion, the voltage value applied to electrodes must exceed a threshold. This phenomenon enables a binary value (i.e., 1/0) to represent a relative logic-high/logic-low value of an actuation voltage, and thus the entire electrode controls can be modeled simply. Furthermore, by patterning electrodes to a general 2D array and adopting time-varying actuations, many droplet-based operations (e.g., mixing and cutting) can be well-performed on a 2D array in a *reconfigurable* manner [22].

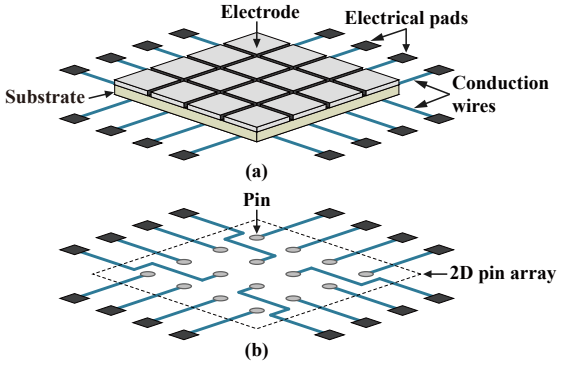
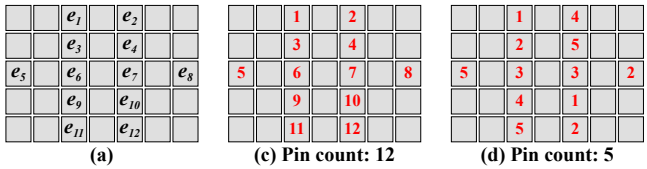


Figure 3. (1) Schematic view of an EWOD chip. (2) Design model on a 2D pin array.

As schematically presented in Figure 3(a), the general diagram of a 2D EWOD chip contains a patterned electrode array, conduction wires, electrical pads, and a substrate [8], [16], [19], [22]. In order to enable the fabrication of smaller and denser electrodes with high interconnect routing flexibility, a typical two-metal-layer design process of EWOD chips is presented in [2], [16]. It comprises two metal layers of 2D electrodes patterned in the first layer and conduction wires routed in the second layer, as well as an inter-insulator of silicon dioxide for via holes patterning. Based on this architecture, design model for EWOD chips can be specified to a 2D pin array, in which signal plan and electrical connections between these pins and electrical pads (i.e., signal ports) are established, as illustrated in Figure 3(b). As a result, the majority of existing efforts can be roughly grouped into two main design steps: 1) electrode addressing and 2) wire routing.

III. Electrode Addressing

Electrode addressing is a method whereby electrodes are addressed with control pins to identify input signals. Early EWOD-chip designs relied on *direct addressing* [8], where each electrode is directly addressed with an independent control pin. This addressing scheme maximizes the flexibility of electrode controls. However, since the control pins are actuated by an external controller which supplies a limited number of signal ports, it is infeasible to actuate a large number of control pins especially for high-density electrode array. For example, the controller in a recently developed chip with over 1000 electrodes for multiplex immunoassay can only actuate 64 control pins [1]. To comply with the limited pin-count supply, *pin-constrained* design of electrode addressing has been introduced as a solution to this problem, which utilizes a limited number of pins to control a large number of electrodes in EWOD chips. A promising solution, *broadcast addressing*, has been presented in [25]. The droplet-controlling information is stored in the form of electrode actuation sequences, where each bit in a sequence represents a signal status ("1"(actuated), "0"(de-actuated), or "X"(don't-care)) of the electrode at a specific time step [25]. Note that the don't-care symbol "X" can be either "1" or "0" which has no impact on scheduled fluidic controls. Examples of an electrode set and their actuation sequences are presented in Figure 4(a) and (b).



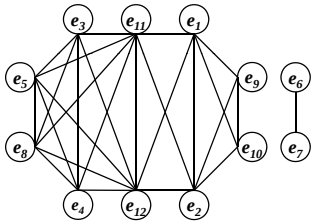
Electrode	e_1	e_2	e_3	e_4	e_5	e_6	e_7	e_8	e_9	e_{10}	e_{11}	e_{12}
Activation Sequence	1	1	0	0	0	X	X	0	X	X	X	X
	0	0	1	1	1	0	0	1	X	X	X	X
	0	0	0	0	0	1	1	0	0	0	X	X
	X	X	0	0	0	0	0	0	1	1	0	0
	X	X	X	X	1	0	0	1	X	X	1	1

(b)

Figure 4. (a) Electrodes that are used for handling fluidic functions. (b) Scheduled fluidic functions in the form of actuation sequences. (c) Applies the direct-addressing scheme. (d) Applies the broadcast-addressing scheme.

Unlike direct addressing, where each electrode is assigned by an independent control pin, broadcast addressing focuses on electrode grouping and control signal merging through the compatibility of actuation sequences. Specifically, each electrode actuation sequence may contain several don't care terms. By carefully replacing these don't care terms with "1" or "0", multiple actuation sequences can be merged to an identical outcome, which is also referred to as the *common compatible sequence* of these electrodes. Therefore, these electrodes can be assigned by the same control pin to receive the same control signal.

Take electrodes e_4 and e_5 in Figure 4(b) for example. By replacing "X" in the actuation sequence of e_4 with "1", we can merge the actuation sequences of e_4 and e_5 to "01001". Therefore, e_4 and e_5 can be addressed with the same control pin due to their mutually compatible actuation sequences. As the example in Figure 4, (c) and (d) respectively demonstrate the direct-addressing and broadcast-addressing outcomes. Compared with the direct-addressing result in (c), the broadcast-addressing result in (d) significantly reduces the required control pins from 12 to 5. This reduction requires fewer electrical devices and connections to perform the same fluidic functions, thus improving chip reliability as well as reducing fabrication cost [25].



(a)

Two electrode grouping results		
Pin	Result 1	Result 2
1	e_1, e_{10}	e_1, e_2
2	e_3, e_8, e_{12}	e_3, e_4, e_8
3	e_6, e_7	e_6, e_7
4	e_2, e_9	e_9, e_{10}
5	e_4, e_5, e_{11}	e_5, e_{11}, e_{12}

(b)

Figure 5. (a) A compatibility graph G_c derived from Figure 4(b). (b) Two possible electrode grouping results.

Researchers have utilized the *compatibility graph* to specify the broadcast addressing [25], where the vertex set represents the electrode set and an edge between two electrodes indicates their corresponding activation sequences are compatible. For example, Figure 5(a) demonstrates a compatibility graph G_c derived from Figure 4(b). Based on the compatibility graph, the electrode grouping can be mapped to the *clique partition problem*, which is a well-known example of an intractable problem in graph theory. Since each clique represents an electrode group with mutually compatible control signals, we can individually assign each clique with a dedicated control pin. Two feasible electrode grouping results can be shown in Figure 5(b). Accordingly, by recognizing a minimum clique partition in the compatibility graph, the required number of control pins can be optimally minimized. However, the general minimum clique partition is known to be NP-hard [9] and thus is computationally expensive.

To resolve the computational cost, many heuristics have been proposed in the literature [24], [25], [26]. The work by [24] proposes an array-partition based method to group the electrode set without introducing unexpected fluidic-level behaviors. The work by [25] presents a greedy method of iterative clique recognitions with maximum cardinality on the compatibility graph. Recent work by [26] applies a connect-5 algorithm to group the electrode set with maximum controlling freedom of a single droplet. Moreover, several works further integrates various pin-count saving techniques into fluidic-level synthesis to achieve design convergence, thereby facilitating pin-count reduction effectively [11], [15], [27].

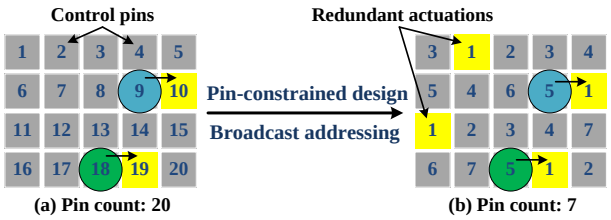


Figure 6. (a) A direct-addressing result uses two pins (pin 10 and pin 19) to generate two exact actuations for moving the two droplets. (b) A broadcast-addressing result uses one pin (pin 1) to generate two exact actuations, plus two redundant actuations, for moving the two droplets.

Although broadcast addressing serves as a promising solution to pin-constrained designs, yet the redundant actuations during signal merging have potentially caused a power-consumption problem. For example, in Figure 6(a), the direct-addressing result needs two exact actuations for moving the two droplets. In Figure 6(b), after applying the broadcast addressing, the pin count is greatly reduced from 20 to 7. Nevertheless, the addressing result needs two exact actuations, plus two *redundant* actuations, for moving the two droplets. As electrodes are controlled in a series of actuation steps, if control pins are not carefully assigned to electrodes, the addressing result will introduce a great number of redundant actuations. Hence, executing a bioassay may incur a high power-consumption problem which is critical to many battery-driven hand-held applications. Regarding this power-consumption problem, one work has been recently proposed to deal with the power-consumption problem incurred from the pin-constrained design [13]. The work by [13] formulates the electrode addressing and power saving into an effective minimum-cost maximum-flow network, with a progressive electrode-addressing scheme for reducing design complexity.

IV. Wire Routing

After electrodes are addressed with control pins, conduction wires must be appropriately routed to establish the correspondence between the control pins (i.e., electrodes with the same pin must be wired together) and the signal pads with a total minimum wirelength. Since signal pads of EWOD chips generally locate outside the component (defined as the 2D pin array) boundary the routing problem that connects these inside terminal pins to outsides signal ports is similar to the typical escape routing problem appearing in many VLSI designs [3]. However, in pin-constrained EWOD-chip designs, multiple electrodes may share the same control pin and therefore a single control signal may actuate multi-terminal pins. To realize the electrical connections, multi-terminal pins with the same control signal must be routed together, and then escape to the component boundary. This feature makes the typical escape router, which is based on the connection of two-terminal pins, unsuitable for the EWOD-chip routing problem. However, readily available CAD tools targeting this type of routing problem are still critically lacking.

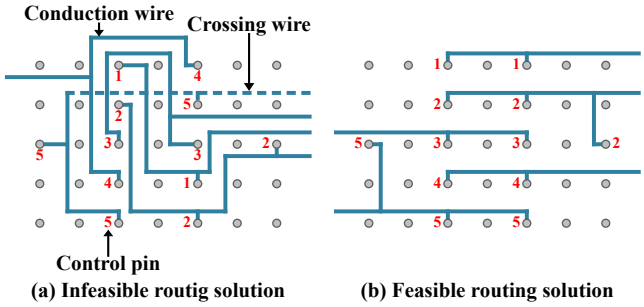


Figure 7. Consideration of electrode addressing and routing: (a) separately; (b) simultaneously.

Regarding the pin-constrained design, a critical problem comes from the interdependence of broadcast addressing and routing. Different broadcast-addressing results lead to different wiring connections and this problem occurs even with the same pin count. If broadcast addressing and routing cannot be considered together, the feasibility and quality of the routing solution may be inevitably limited. For example, Figure 7 illustrates two routing solutions under two different design methods that perform the same fluidic controls (the corresponding electrode groups and addressing results can refer to the result 1 and result 2 in Figure 5(b), respectively). In (a), the separate consideration of electrode addressing and routing confronts many back detours for pins 3-4, and thus blocks the routing for pin 5. On the other hand, in (b), simultaneous consideration of electrode addressing and routing provides a higher feasibility and quality routing solution in terms of routability and wirelength. In the case of (a), additional post processes such as electrode readdressing and rerouting or even a multi-layer routing structure should be considered. Regarding this, an effective design to low-cost manufacturing of electrical connections cannot be realized [8].

There is only one existing work proposed in [11] that considers the an automated design of EWOD-chip routing. The work by [11]

simultaneously solves the electrode addressing and routing by adopting a two-stage technique of global routing followed by progressive routing. In global routing, a set of horizontal/vertical global routing tracks is constructed using a maximum-flow formulation. By guiding straight routes on these tracks, the pin count and wirelength can be simultaneously minimized in a global view. Then, the progressive routing iteratively completes the addressing and routing with respect to these tracks using a minimum-cost maximum-flow model, while maintaining a minimum growth of pin count and wirelength between successive iterations.

V. Future Design Challenges

A number of open problems remain to be tackled in the development of CAD tools for chip-level designs and optimizations of DMFBs. One significant problem is the reliability problem incurred from pin-constrained designs. Control-pin/-signal sharing might introduce additional and unnecessary electrode actuations, which has the potential to make an electrode confront excessive actuations in case of a naive design. Studies on EWOD chips have reported this kind of problem accelerates the extent of trapping charge, leading to a permanent degradation of dielectric layer [5], [14], [23]. This scenario inevitably impedes complete and correct fluidic controls and therefore degrades the chip reliability. Thus, it becomes desirable and crucial to strike a balance between control-pin/-signal sharing and reliability preservation when the chip size and assay functionality grow, particularly under the circumstance of pin-constrained design.

Besides, modern EWOD-chip design needs to consider several on-chip obstacles which are incurred from permanently embedded devices for the executions of specific fluidic protocols [6]. For example, a DNA sequencing chip may embed several electrophoresis devices for fast and accurate sample isolation [7], [18]. As these devices are independent from EWOD actuations, they are typically regarded as on-chip obstacles. These obstacles add significant complexity to the design of EWOD chips, especially for wire routing, as conduction wires should avoid routing through/across these obstacles for correct signal transmission.

Optimization in energy domains also needs to be investigated. Such optimization problems that span several energy domains (e.g., electrical, circuit, fluidic, and thermal domains) appear to be extremely difficult due to the further involvements of energy-related constraints or objectives. For example, we should limit the fanout of a single control pin to avoid overly charge sharing, which might cause problems such as high power dissipation, trapped charge, and so on.

As a consequence, effective and efficient solutions to all the above discussions are critically essential to ensure the quality of biochips designed through the assistance of CAD approaches.

VI. Conclusions

In this paper, we have presented the optimization problems arising in the automated chip-level design of DMFBs. We have focused on EWOD-chip designs and addressed two major design steps of electrode addressing and wire routing, as well as providing a comprehensive technical survey on related CAD tools. Several associative optimization problems appearing in the design of electrode addressing and wire routing are investigated as well. In addition, we have pointed out a set of open problems that remain to be tackled in the future. The authors believe this paper will spark more research interests being devoted into the developments of CAD tools particularly for EWOD-chip designs, thereby bridging the current gap between automated fluidic-level synthesis and chip-level design.

Acknowledgment

This work was partially supported by the National Science Council of Taiwan ROC under Grant No. NSC 99-2220-E-006-005, 99-2221-E-006-220, and 100-2220-E-006-016.

References

[1] Advanced Liquid Logic, Inc., http://www.liquid-logic.com.

[2] Microfluidic Lab., Duke University, http://microfluidics.ee.duke.edu/

[3] C. J. Alpert, D. P. Mehta, S. S. Sapatnekar, "Handbook of Algorithms for Physical Design Automation," CRC Press, 2009.

[4] K. Chakrabarty, "Towards fault-tolerant digital microfluidic lab-on-chip: defects, fault modeling, testing, and reconfiguration," *Proc. IEEE ICBCS*, pp. 329–332, 2008.

[5] A. I. Drygiannakis, A. G. Papathanasiou, and A. G. Boudouvis, "On the connection between dielectric breakdown strength, trapping of charge, and contact angle saturation in electrowetting," *ACS J. Langmuir*, no. 25, pp. 147–152, 2009.

[6] R. B. Fair, "Digital microfluidics: Is a true lab-on-a-chip possible?" *Microfluidics and Nanofluidics*, vol. 3, pp. 245–281, 2007

[7] R. B. Fair, A. Khlystov, T. D. Tailor, V. Ivanov, R. D. Evans, P. B. Griffin, S. Vijay, V. K. Pamula, M. G. Pollack, and J. Zhou, "Chemical and Biological Applications of Digital-Microfluidic Devices," *IEEE Design and Test*, vol. 24, pp. 20–24, 2007

[8] J. Gong and C. J. Kim, "Direct-referencing two-dimensional-array digital microfluidics using multilayer printed circuit board," *IEEE J. MEMS*, no. 2, pp. 257–264, 2008.

[9] J. L. Gross, and J. Yellen, "Graph Theory and Its Application," CRC Press, FL, 1999.

[10] T.-Y. Ho, J. Zeng, and K. Chakrabarty, "Digital microfluidic biochips: A vision for functional diversity and more than Moore," *Proc. IEEE/ACM ICCAD*, pp. 578–585, 2010.

[11] T.-W. Huang and T.-Y. Ho, "A two-stage ILP-based droplet routing for pin-constrained digital microfluidic biochips," *Proc. ACM ISPD*, pp. 201–208, 2010

[12] T.-W. Huang, S.-Y. Yeh, and T.-Y. Ho, "A network-flow based pin-count aware routing algorithm for broadcast electrode-addressing EWOD chips," *Proc. IEEE/ACM ICCAD*, pp. 425–431, 2010

[13] T.-W. Huang, H.-Y. Su, and T.-Y. Ho, "Progressive network-flow based power-aware broadcast addressing for pin-constrained digital microfluidic biochips," *Proc. IEEE/ACM DAC*, 2011

[14] A. Kerber, F. Cartier, R. Degraeve, P. J. Roussel, L. Pantisano, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke, "Charge trapping and dielectric reliability of SiO2-Al2O3 gate stacks with TiN electrodes," *IEEE Trans. on Electron Devices*, no. 50, pp. 1261–1269, 2003.

[15] C. C.-Y. Lin and Y.-W. Chang, "ILP-based pin-count aware design methodology for microfluidic biochips," *Proc. IEEE/ACM DAC*, pp. 258–263, 2009.

[16] Y.-Y. Lin, R. D. Evans, E. Welch, B.N. Hsu, A. C. Madison, and R. B. Fair, "Low Voltage Electrowetting-on-Dielectric Platform using Multi-Layer Insulators.," *Sensors and Actuators B: Chemical*, pp. 465–470, 2010.

[17] M. G. Pollack, A. D. Shenderov, and R. B. Fair, "Electrowetting-based actuation of droplets for integrated microfluidics," *LOC*, pp. 96–101, 2002.

[18] R. Sista, Z. Hua, P. Thwar, A. Sudarsan, V. Srinivasan, A. E. Eckhardt, M. Pollack, and V. Pamula, "Development of a digital microfluidic platform for point of care testing," *Lab on chip*, no. 8, pp. 2091–2104, 2008.

[19] J. H. Song, R. Evans, Y. Y. Lin, B. N. Hsu, and R. B. Fair, "A scaling model for electrowetting-on-dielectric microfluidic actuators," *Microfluidics and Nanofluidics*, pp. 75–89, 2009.

[20] F. Su and K. Chakrabarty, "Architectural-level synthesis of digital microfluidics-based biochips," *Proc. IEEE/ACM ICCAD*, pp. 223–228, 2004.

[21] F. Su and K. Chakrabarty, "Unified high-level synthesis and module placement for defect-tolerant microfluidic biochips," *IEEE/ACM DAC*, pp. 825–830, 2005.

[22] F. Su, K. Chakrabarty, and R. B. Fair, "Microfluidics based biochips: Technology issues, implementation platforms, and design-automation challenges," *IEEE Trans. on CAD*, pp. 211–223, 2006.

[23] H. J. J. Verheijen and M. W. J. Prins, "Reversible electrowetting and trapping of charge: model and experiments," *ACS J. Langmuir*, no. 15, pp. 6616–6620, 1999.

[24] T. Xu and K. Chakrabarty, "Droplet-trace-based array partitioning and a pin assignment algorithm for the automated design of digital microfluidic biochips," *Proc. CODES+ISSS*, pp. 112–117, 2006.

[25] T. Xu and K. Chakrabarty, "Broadcast electrode-addressing for pin-constrained multi-functional digital microfluidic biochips," *Proc. IEEE/ACM DAC*, pp. 173–178, 2008.

[26] T. Xu, K. Chakrabarty and V. K. Pamula, "Defect-tolerant design and optimization of a digital microfluidic biochip for protein crystallization," *IEEE Trans. on CAD*, 2010.

[27] Y. Zhao and K. Chakrabarty, "Co-optimization of droplet routing and pin assignment in disposable digital microfluidic biochips," *Proc. ACM ISPD*, pp. 69–76, 2011.